# 2-Mbit (64K x 32) Flow-Through Sync SRAM

## Features

- **64K x 32 common I/O**
- **3.3V core power supply**
- **3.3V I/O supply**
- **Fast clock-to-output times**
  - **— 6.5 ns (133-MHz version)**
  - **— 8.0 ns (100-MHz version)**
- **Provide high-performance 2-1-1-1 access rate**
- **User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences**
- **Separate processor and controller address strobes**
- **Synchronous self-timed write**
- **Asynchronous output enable**
- **Supports 3.3V I/O level**
- **Offered in JEDEC-standard lead-free 100-pin TQFP package**
- **"ZZ" Sleep Mode option**

## Functional Description[1]

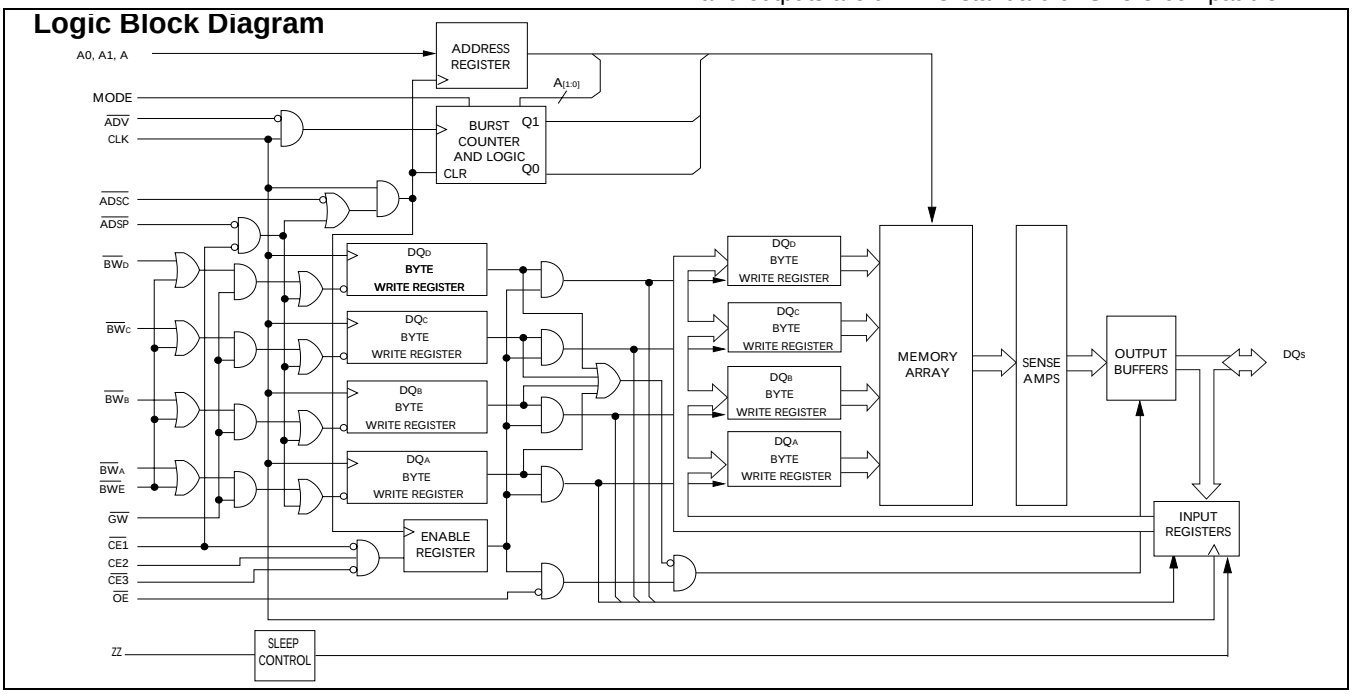
The CY7C1336H is a 64K x 32 synchronous cache RAM designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133-MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($CE_1$), depth-expansion Chip Enables ($CE_2$ and $CE_3$), Burst Control inputs (ADSC, ADSP, and ADV), Write Enables ($BW_{[A:D]}$, and BWE), and Global Write (GW). Asynchronous inputs include the Output Enable (OE) and the ZZ pin.

The CY7C1336H allows either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the Processor Address Strobe (ADSP) or the cache Controller Address Strobe (ADSC) inputs. Address advancement is controlled by the Address Advancement (ADV) input.

Addresses and chip enables are registered at rising edge of clock when either Address Strobe Processor (ADSP) or Address Strobe Controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin (ADV).

The CY7C1336H operates from a +3.3V core power supply while all outputs may operate with a +3.3V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

## Logic Block Diagram



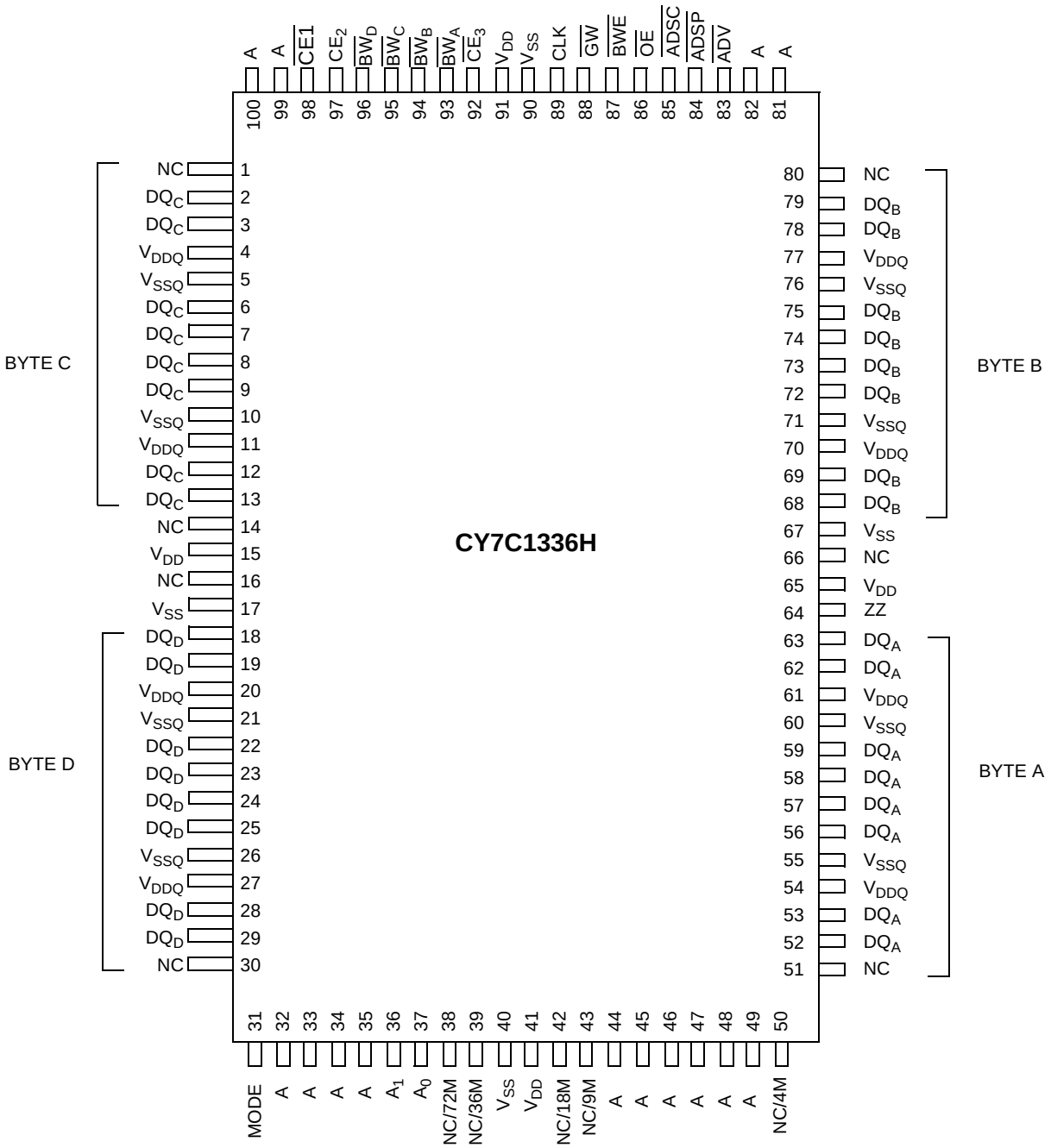

**Note:**
1. For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

## Selection Guide

| | 133 MHz | 100 MHz | Unit |
|---|---|---|---|
| Maximum Access Time | 6.5 | 8.0 | ns |
| Maximum Operating Current | 225 | 205 | mA |
| Maximum Standby Current | 40 | 40 | mA |

## Pin Configuration

**100-pin TQFP Pinout**






[+] Feedback

## Pin Definitions

| Name | I/O | Description |
|---|---|---|
| A0, A1, A | Input-Synchronous | **Address Inputs used to select one of the 64K address locations**. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1$, $CE_2$, and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter. |
| $\overline{BW}_A$, $\overline{BW}_B$ $\overline{BW}_C$, $\overline{BW}_D$ | Input-Synchronous | **Byte Write Select Inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct Byte Writes to the SRAM. Sampled on the rising edge of CLK. |
| $\overline{GW}$ | Input-Synchronous | **Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global Write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_{[A:D]}$ and $\overline{BWE}$). |
| $\overline{BWE}$ | Input-Synchronous | **Byte Write Enable Input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a Byte Write. |
| CLK | Input-Clock | **Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation. |
| $\overline{CE}_1$ | Input-Synchronous | **Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $CE_2$ and $\overline{CE}_3$ to select/deselect the device. ADSP is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded. |
| $CE_2$ | Input-Synchronous | **Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device. $CE_2$ is sampled only when a new external address is loaded. |
| $\overline{CE}_3$ | Input-Synchronous | **Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $CE_2$ to select/deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded. |
| $\overline{OE}$ | Input-Asynchronous | **Output Enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a Read cycle when emerging from a deselected state. |
| $\overline{ADV}$ | Input-Synchronous | **Advance Input signal, sampled on the rising edge of CLK**. When asserted, it automatically increments the address in a burst cycle. |
| $\overline{ADSP}$ | Input-Synchronous | **Address Strobe from Processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH |
| $\overline{ADSC}$ | Input-Synchronous | **Address Strobe from Controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. |
| ZZ | Input-Asynchronous | **ZZ "sleep" Input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down. |
| DQs | I/O-Synchronous | **Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the Read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs are placed in a tri-state condition. |
| $V_{DD}$ | Power Supply | **Power supply inputs to the core of the device**. |
| $V_{SS}$ | Ground | **Ground for the core of the device**. |
| $V_{DDQ}$ | I/O Power Supply | **Power supply for the I/O circuitry**. |
| $V_{SSQ}$ | I/O Ground | **Ground for the I/O circuitry**. |
| MODE | Input-Static | **Selects Burst Order**. When tied to GND selects linear burst sequence. When tied to $V_{DD}$ or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up. |
| NC | | **No Connects**. Not Internally connected to the die. 4M, 9M, 18M, 72M, 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die. |



[+] Feedback

## Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ($t_{CDV}$) is 6.5 ns (133-MHz device).

The CY7C1336H supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte Write operations are qualified with the Byte Write Enable ($BW_E$) and Byte Write Select ($BW_{[A:D]}$) inputs. A Global Write Enable (GW) overrides all Byte Write inputs and writes data to all four bytes. All Writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE_1}$, $CE_2$, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

### Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, $CE_2$, and $\overline{CE_3}$ are all asserted active, and (2) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW (if the access is initiated by $\overline{ADSC}$, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the $\overline{OE}$ input is asserted LOW, the requested data will be available at the data outputs a maximum to $t_{CDV}$ after clock rise. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

### Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, $CE_2$, $\overline{CE_3}$ are all asserted active, and (2) $\overline{ADSP}$ is asserted LOW. The addresses presented are loaded into the address register and the burst inputs (GW, $BW_E$, and $BW_{[A:D]}$) are ignored during this first clock cycle. If the Write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a Write) on the next clock rise, the appropriate data will be latched and written into the device. Byte Writes are allowed. During Byte Writes, $BW_A$ controls $DQ_A$ and $BW_B$ controls $DQ_B$, $BW_C$ controls $DQ_C$, and $BW_D$ controls $DQ_D$. All I/Os are tri-stated during a Byte Write. Since this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a Write cycle is detected, regardless of the state of $\overline{OE}$.

### Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, $CE_2$, and $\overline{CE_3}$ are all asserted active, (2) $\overline{ADSC}$ is asserted LOW, (3) $\overline{ADSP}$ is deasserted HIGH, and (4) the Write input signals (GW, $BW_E$, and $BW_{\overline{[A:D]}}$) indicate a write access. $\overline{ADSC}$ is ignored if $\overline{ADSP}$ is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to $DQ_{[D:A]}$ will be written into the specified address location. Byte Writes are allowed. During Byte Writes, $BW_A$ controls $DQ_A$, $BW_B$ controls $DQ_B$, $BW_C$ controls $DQ_C$, and $BW_D$ controls $DQ_D$. All I/Os are tri-stated when a Write is detected, even a Byte Write. Since this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/Os must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a Write cycle is detected, regardless of the state of $\overline{OE}$.

### Burst Sequences

The CY7C1336H provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE will select a linear burst sequence. A HIGH on MODE will select an interleaved burst order. Leaving MODE unconnected will cause the device to default to a interleaved burst sequence.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. CEs, ADSP, and ADSC must remain inactive for the duration of $t_{ZZREC}$ after the ZZ input returns LOW.

## Interleaved Burst Address Table (MODE = Floating or $V_{DD}$)

| First Address A1, A0 | Second Address A1, A0 | Third Address A1, A0 | Fourth Address A1, A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

## Linear Burst Address Table (MODE = GND)

| First Address $A_1, A_0$ | Second Address $A_1, A_0$ | Third Address $A_1, A_0$ | Fourth Address $A_1, A_0$ |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 10 | 11 | 00 |
| 10 | 11 | 00 | 01 |
| 11 | 00 | 01 | 10 |



[+] Feedback

## ZZ Mode Electrical Characteristics

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DDZZ}$ | Sleep mode standby current | ZZ ≥ $V_{DD}$ – 0.2V | | 40 | mA |
| $t_{ZZS}$ | Device operation to ZZ | ZZ ≥ $V_{DD}$ – 0.2V | | $2t_{CYC}$ | ns |
| $t_{ZZREC}$ | ZZ recovery time | ZZ ≤ 0.2V | $2t_{CYC}$ | | ns |
| $t_{ZZI}$ | ZZ Active to sleep current | This parameter is sampled | | $2t_{CYC}$ | ns |
| $t_{RZZI}$ | ZZ Inactive to exit sleep current | This parameter is sampled | 0 | | ns |

## Truth Table [2, 3, 4, 5, 6]

| Cycle Description | ADDRESS Used | $\overline{CE_1}$ | $CE_2$ | $\overline{CE_3}$ | ZZ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{WRITE}$ | $\overline{OE}$ | CLK | DQ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Deselected Cycle, Power-down | None | H | X | X | L | X | L | X | X | X | L-H | Tri-State |
| Deselected Cycle, Power-down | None | L | L | X | L | L | X | X | X | X | L-H | Tri-State |
| Deselected Cycle, Power-down | None | L | X | H | L | L | X | X | X | X | L-H | Tri-State |
| Deselected Cycle, Power-down | None | L | L | X | L | H | L | X | X | X | L-H | Tri-State |
| Deselected Cycle, Power-down | None | X | X | X | L | H | L | X | X | X | L-H | Tri-State |
| Sleep Mode, Power-down | None | X | X | X | H | X | X | X | X | X | X | Tri-State |
| Read Cycle, Begin Burst | External | L | H | L | L | L | X | X | X | L | L-H | Q |
| Read Cycle, Begin Burst | External | L | H | L | L | L | X | X | X | H | L-H | Tri-State |
| Write Cycle, Begin Burst | External | L | H | L | L | H | L | X | L | X | L-H | D |
| Read Cycle, Begin Burst | External | L | H | L | L | H | L | X | H | L | L-H | Q |
| Read Cycle, Begin Burst | External | L | H | L | L | H | L | X | H | H | L-H | Tri-State |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | L | L-H | Q |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | H | L-H | Tri-State |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | L | L-H | Q |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | H | L-H | Tri-State |
| Write Cycle, Continue Burst | Next | X | X | X | L | H | H | L | L | X | L-H | D |
| Write Cycle, Continue Burst | Next | H | X | X | L | X | H | L | L | X | L-H | D |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | L | L-H | Q |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | H | L-H | Tri-State |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | L | L-H | Q |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | H | L-H | Tri-State |
| Write Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | L | X | L-H | D |
| Write Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | L | X | L-H | D |

**Notes:**

2. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
3. $\overline{WRITE}$ = L when any one or more Byte Write Enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$) and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte Write Enable signals ($BW_A$, $BW_B$, $BW_C$, $BW_D$), BWE, GW = H.
4. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. The SRAM always initiates a Read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_{[A:D]}}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the Write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the Write cycle.
6. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during Write cycles. During a Read cycle all data bits are Tri-State when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).



[+] Feedback

## Truth Table for Read/Write[2, 3]

| Function | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BW_D}$ | $\overline{BW_C}$ | $\overline{BW_B}$ | $\overline{BW_A}$ |
|---|---|---|---|---|---|---|
| Read | H | H | X | X | X | X |
| Read | H | L | H | H | H | H |
| Write Byte (A, $DQP_A$) | H | L | H | H | H | L |
| Write Byte (B, $DQP_B$) | H | L | H | H | L | H |
| Write Bytes (B, A, $DQP_A$, $DQP_B$) | H | L | H | H | L | L |
| Write Byte (C, $DQP_C$) | H | L | H | L | H | H |
| Write Bytes (C, A, $DQP_C$, $DQP_A$) | H | L | H | L | H | L |
| Write Bytes (C, B, $DQP_C$, $DQP_B$) | H | L | H | L | L | H |
| Write Bytes (C, B, A, $DQP_C$, $DQP_B$, $DQP_A$) | H | L | H | L | L | L |
| Write Byte (D, $DQP_D$) | H | L | L | H | H | H |
| Write Bytes (D, A, $DQP_D$, $DQP_A$) | H | L | L | H | H | L |
| Write Bytes (D, B, $DQP_D$, $DQP_A$) | H | L | L | H | L | H |
| Write Bytes (D, B, A, $DQP_D$, $DQP_B$, $DQP_A$) | H | L | L | H | L | L |
| Write Bytes (D, B, $DQP_D$, $DQP_B$) | H | L | L | L | H | H |
| Write Bytes (D, B, A, $DQP_D$, $DQP_C$, $DQP_A$) | H | L | L | L | H | L |
| Write Bytes (D, C, A, $DQP_D$, $DQP_B$, $DQP_A$) | H | L | L | L | L | H |
| Write All Bytes | H | L | L | L | L | L |
| Write All Bytes | L | X | X | X | X | X |



[+] Feedback

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on $V_{DD}$ Relative to GND..... –0.5V to +4.6V

DC Voltage Applied to Outputs in Tri-State..... –0.5V to $V_{DDQ}$ + 0.5V

DC Input Voltage.....–0.5V to $V_{DD}$ + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

## Operating Range

| Range | Ambient Temperature] | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 3.3V –5%/+10% | 3.3V –5% to $V_{DD}$ |
| Industrial | –40°C to +85°C | | |

## Electrical Characteristics Over the Operating Range [7, 8]

| Parameter | Description | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | | 3.135 | 3.6 | V |
| $V_{DDQ}$ | I/O Supply Voltage | | | 3.135 | 3.6 | V |
| $V_{OH}$ | Output HIGH Voltage | for 3.3V I/O, $I_{OH}$ = –4.0 mA | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | for 3.3V I/O, $I_{OL}$ = 8.0 mA | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | for 3.3V I/O | | 2.0 | $V_{DD}$ + 0.3V | V |
| $V_{IL}$ | Input LOW Voltage[7] | for 3.3V I/O | | –0.3 | 0.8 | V |
| $I_X$ | Input Leakage Current except ZZ and MODE | GND ≤ $V_I$ ≤ $V_{DDQ}$ | | –5 | 5 | µA |
| | Input Current of MODE | Input = $V_{SS}$ | | –30 | | µA |
| | | Input = $V_{DD}$ | | | 5 | µA |
| | Input Current of ZZ | Input = $V_{SS}$ | | –5 | | µA |
| | | Input = $V_{DD}$ | | | 30 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_I$ ≤ $V_{DDQ}$, Output Disabled | | –5 | 5 | µA |
| $I_{DD}$ | $V_{DD}$ Operating Supply Current | $V_{DD}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$= 1/$t_{CYC}$ | 7.5-ns cycle, 133 MHz | | 225 | mA |
| | | | 10-ns cycle, 100 MHz | | 205 | mA |
| $I_{SB1}$ | Automatic CE Power-Down Current—TTL Inputs | Max. $V_{DD}$, Device Deselected, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$, inputs switching | 7.5-ns cycle, 133 MHz | | 90 | mA |
| | | | 10-ns cycle, 100 MHz | | 80 | mA |
| $I_{SB2}$ | Automatic CE Power-Down Current—CMOS Inputs | Max. $V_{DD}$, Device Deselected, $V_{IN}$ ≥ $V_{DD}$ – 0.3V or $V_{IN}$ ≤ 0.3V, f = 0, inputs static | All speeds | | 40 | mA |
| $I_{SB3}$ | Automatic CE Power-Down Current—CMOS Inputs | Max. $V_{DD}$, Device Deselected, $V_{IN}$ ≥ $V_{DDQ}$ – 0.3V or $V_{IN}$ ≤ 0.3V, f = $f_{MAX}$, inputs switching | 7.5-ns cycle, 133 MHz | | 75 | mA |
| | | | 10-ns cycle, 100 MHz | | 65 | mA |
| $I_{SB4}$ | Automatic CE Power-Down Current—TTL Inputs | Max. $V_{DD}$, Device Deselected, $V_{IN}$ ≥ $V_{DD}$ – 0.3V or $V_{IN}$ ≤ 0.3V, f = 0, inputs static | All speeds | | 45 | mA |

**Notes:**
7. Overshoot: $V_{IH}$(AC) < $V_{DD}$ +1.5V (Pulse width less than $t_{CYC}$/2), undershoot: $V_{IL}$(AC) > –2V (Pulse width less than $t_{CYC}$/2).
8. $T_{Power\text{-}up}$: Assumes a linear ramp from 0v to $V_{DD}$(min.) within 200 ms. During this time $V_{IH}$ < $V_{DD}$ and $V_{DDQ}$ ≤ $V_{DD}$.



[+] Feedback

## Capacitance[9]

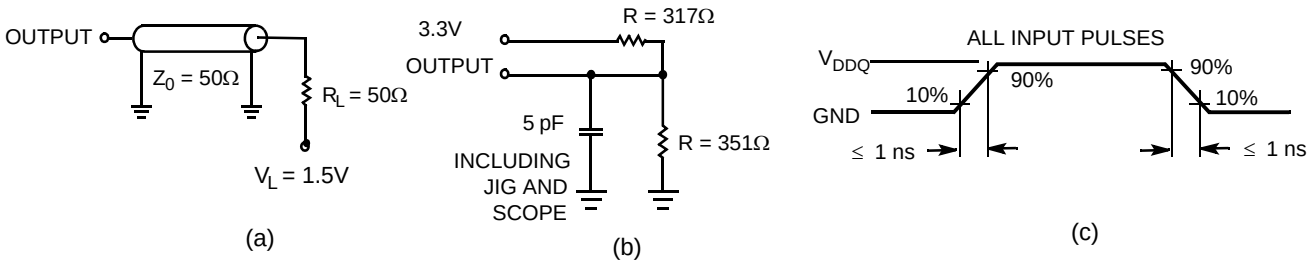
| Parameter | Description | Test Conditions | 100 TQFP Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{DD}$ = 3.3V, $V_{DDQ}$ = 3.3V | 5 | pF |
| $C_{CLK}$ | Clock Input Capacitance | | 5 | pF |
| $C_{I/O}$ | Input/Output Capacitance | | 5 | pF |

## Thermal Resistance[9]

| Parameter | Description | Test Conditions | 100 TQFP Package | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51 | 30.32 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 6.85 | °C/W |

## AC Test Loads and Waveforms

### 3.3V I/O Test Load




**Note:**
9. Tested initially and after any design or process change that may affect these parameters.



[+] Feedback

## Switching Characteristics Over the Operating Range [10, 11]

| Parameter | Description | 133 MHz | | 100 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{POWER}$ | $V_{DD}$(Typical) to the First Access[12] | 1 | | 1 | | ms |
| **Clock** | | | | | | |
| $t_{CYC}$ | Clock Cycle Time | 7.5 | | 10 | | ns |
| $t_{CH}$ | Clock HIGH | 2.5 | | 4.0 | | ns |
| $t_{CL}$ | Clock LOW | 2.5 | | 4.0 | | ns |
| **Output Times** | | | | | | |
| $t_{CDV}$ | Data Output Valid after CLK Rise | | 6.5 | | 8.0 | ns |
| $t_{DOH}$ | Data Output Hold after CLK Rise | 2.0 | | 2.0 | | ns |
| $t_{CLZ}$ | Clock to Low-Z[13, 14, 15] | 0 | | 0 | | ns |
| $t_{CHZ}$ | Clock to High-Z[13, 14, 15] | | 3.5 | | 3.5 | ns |
| $t_{OEV}$ | $\overline{OE}$ LOW to Output Valid | | 3.5 | | 3.5 | ns |
| $t_{OELZ}$ | $\overline{OE}$ LOW to Output Low-Z[13, 14, 15] | 0 | | 0 | | ns |
| $t_{OEHZ}$ | $\overline{OE}$ HIGH to Output High-Z[13, 14, 15] | | 3.5 | | 3.5 | ns |
| **Set-up Times** | | | | | | |
| $t_{AS}$ | Address Set-up before CLK Rise | 1.5 | | 2.0 | | ns |
| $t_{ADS}$ | $\overline{ADSP}$, $\overline{ADSC}$ Set-up before CLK Rise | 1.5 | | 2.0 | | ns |
| $t_{ADVS}$ | $\overline{ADV}$ Set-up before CLK Rise | 1.5 | | 2.0 | | ns |
| $t_{WES}$ | $\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:D]}$ Set-up before CLK Rise | 1.5 | | 2.0 | | ns |
| $t_{DS}$ | Data Input Set-up before CLK Rise | 1.5 | | 2.0 | | ns |
| $t_{CES}$ | Chip Enable Set-up | 1.5 | | 2.0 | | ns |
| **Hold Times** | | | | | | |
| $t_{AH}$ | Address Hold after CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{ADH}$ | $\overline{ADSP}$, $\overline{ADSC}$ Hold after CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{WEH}$ | $\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:D]}$ Hold after CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{ADVH}$ | $\overline{ADV}$ Hold after CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{DH}$ | Data Input Hold after CLK Rise | 0.5 | | 0.5 | | ns |
| $t_{CEH}$ | Chip Enable Hold after CLK Rise | 0.5 | | 0.5 | | ns |

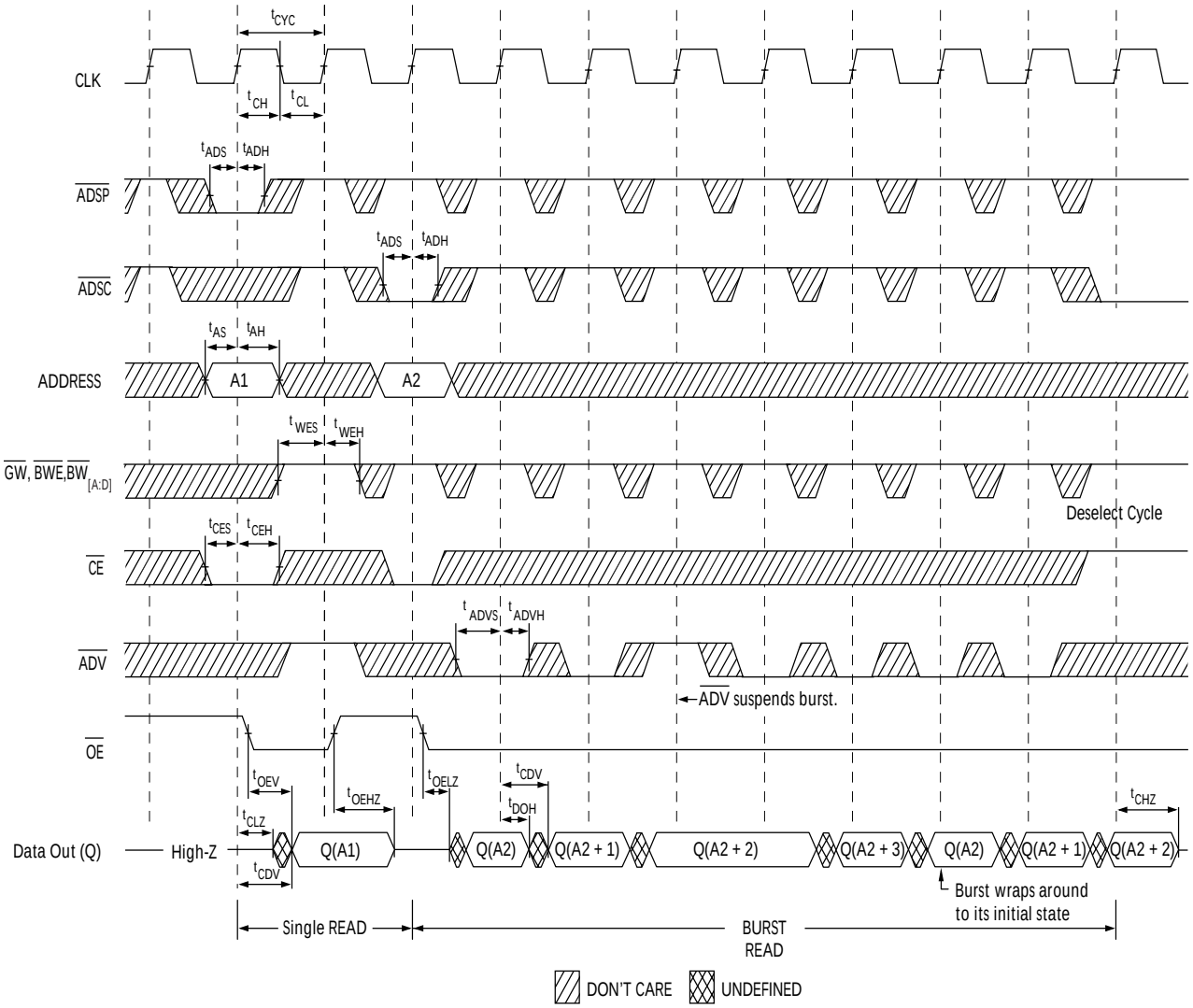
**Notes:**
10. Timing reference level is 1.5V when $V_{DDQ}$ = 3.3V.
11. Test conditions shown in (a) of AC Test Loads unless otherwise noted.
12. This part has a voltage regulator internally; $t_{POWER}$ is the time that the power needs to be supplied above $V_{DD}$(minimum) initially before a Read or Write operation can be initiated.
13. $t_{CHZ}$, $t_{CLZ}$,$t_{OELZ}$, and $t_{OEHZ}$ are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
14. At any given voltage and temperature, $t_{OEHZ}$ is less than $t_{OELZ}$ and $t_{CHZ}$ is less than $t_{CLZ}$ to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
15. This parameter is sampled and not 100% tested.



[+] Feedback

## Timing Diagrams

### Read Cycle Timing[16]



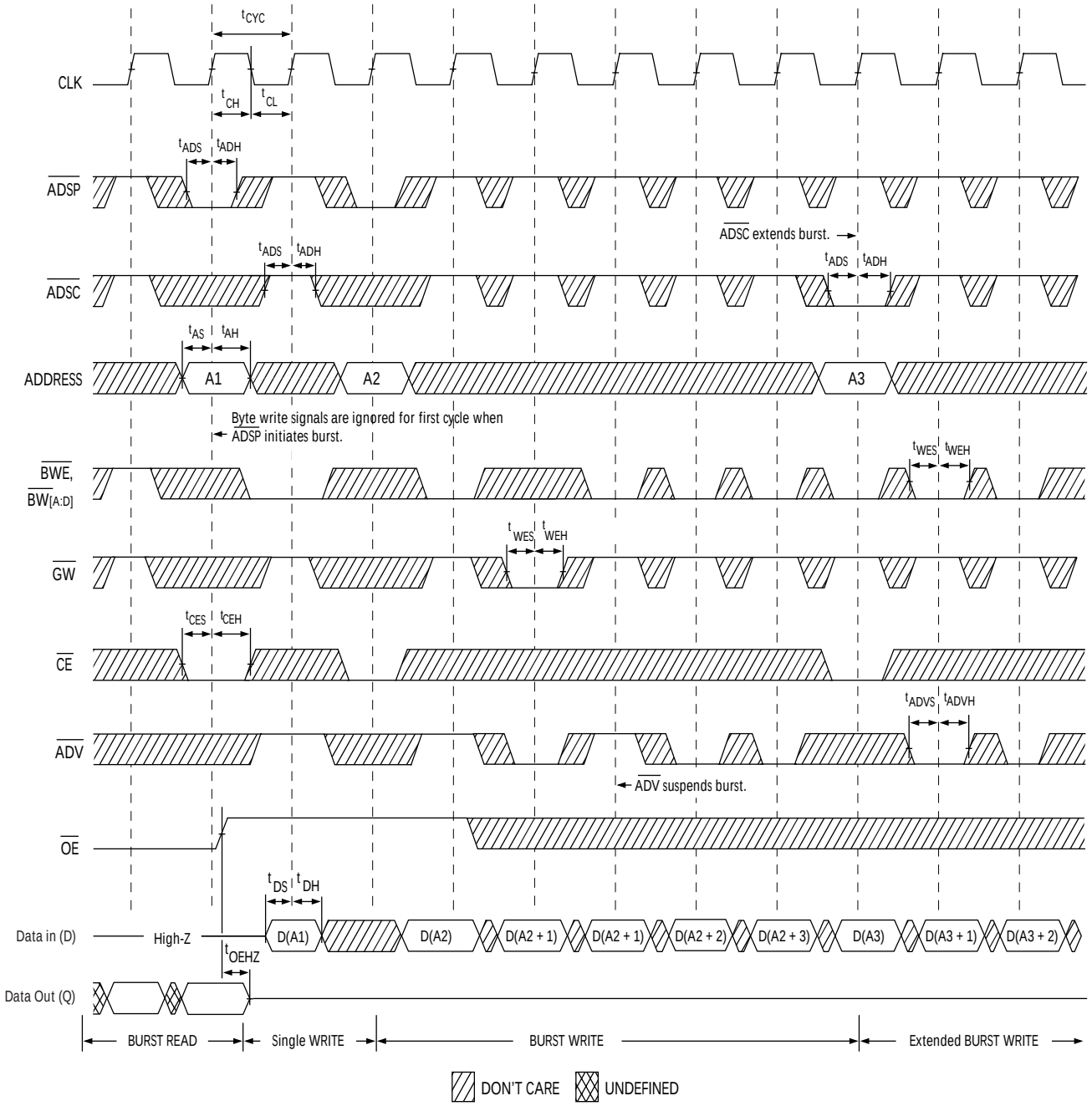

**Note:**
16. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, $CE_2$ is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or $CE_2$ is LOW or $\overline{CE}_3$ is HIGH.



[+] Feedback

## Timing Diagrams (continued)

### Write Cycle Timing[16, 17]




**Note:**
17. Full width Write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_{[A:D]}$ LOW.



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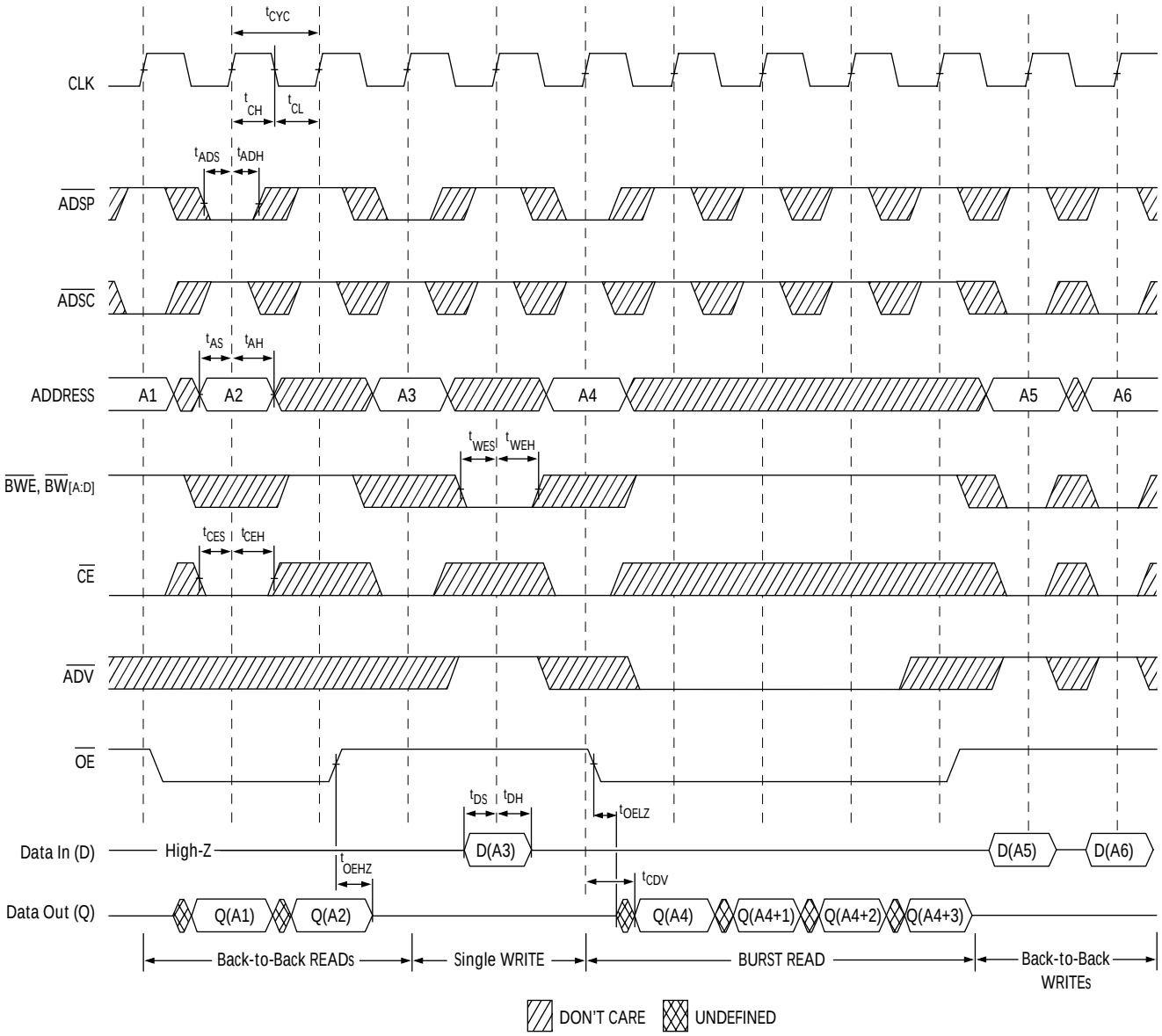
## Timing Diagrams (continued)

### Read/Write Timing[16, 18, 19]



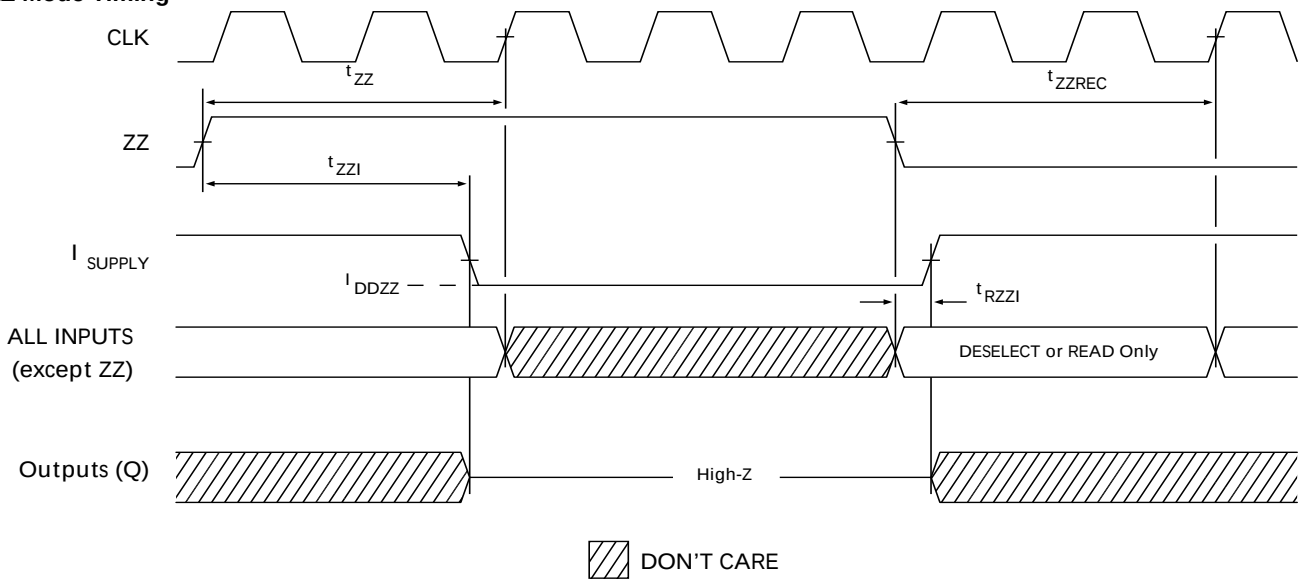

**Notes:**
18. The data bus (Q) remains in High-Z following a Write cycle unless an ADSP, ADSC, or ADV cycle is performed.
19. GW is HIGH.



[+] Feedback

## Timing Diagrams (continued)

### ZZ Mode Timing[20, 21]




**Notes:**
20. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
21. DQs are in High-Z when exiting ZZ sleep mode.



[+] Feedback

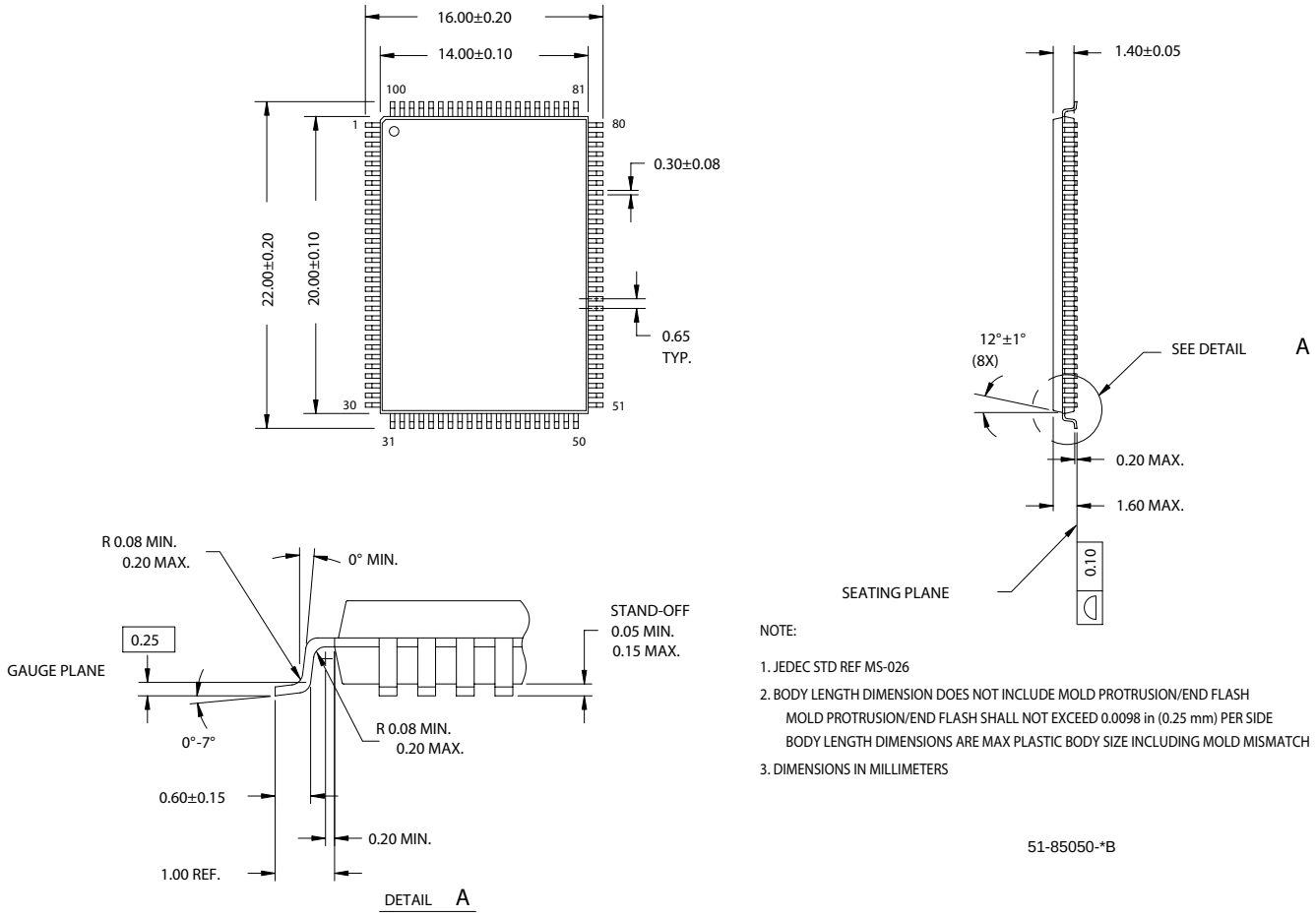
## Ordering Information

| Speed (MHz) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 133 | CY7C1336H-133AXC | 51-85050 | 100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free | Commercial |
| | CY7C1336H-133AXI | 51-85050 | 100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free | Industrial |
| 100 | CY7C1336H-100AXC | 51-85050 | 100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free | Commercial |
| | CY7C1336H-100AXI | 51-85050 | 100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Lead-Free | Industrial |

Please contact your local Cypress sales representative for availability of these parts.

## Package Diagram

**100-pin TQFP (14 x 20 x 1.4 mm) (51-85050)**

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## Document History Page

| Document Title: CY7C1336H 2-Mbit (64K x 32) Flow-Through Sync SRAM<br>Document Number: 001-00210 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 347377 | See ECN | PCI | New Data Sheet |
| *A | 428408 | See ECN | NXR | Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court”<br>Changed Three-State to Tri-State.<br>Modified “Input Load” to “Input Leakage Current except ZZ and MODE” in the Electrical Characteristics Table.<br>Modified test condition from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$<br>Replaced Package Name column with Package Diagram in the Ordering Information table.<br>Replaced Package Diagram of 51-85050 from *A to *B |



[+] Feedback